

Design and Building of a 300W MOSFET Push-Pull Power Amplifier for 144MHz

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1. Introduction

Although valves are quite a common choice amongst the amateur community for building (high) power amplifiers, I opted for building a MOSFET Solid-State Power Amplifier (SSPA) instead. For 144 MHz I am using a remote transverter located close to my antenna tower, so I preferred to build a low voltage amplifier, in order to avoid setting-up a remote high voltage power supply. Here are the advantages and drawbacks of solid-state power amplifiers.

Advantages:

- No high voltage
- No heat-up time
- Less mechanical machining
- Lightweight equipment, easy to carry
- No retune needed (thermal drift)
- High MTBF.

Drawbacks:

- Limited amount of power, unless paralleling amplifiers
- Expensive transistors
- The MOSFET Gate is sensitive to electrostatic charges

The goal of this article is not only to describe such an amplifier, but also to provide experimental guidelines to design a push-pull MOSFET amplifier. The one described here is narrowband and provides more than 250 W RF power, for a current consumption of 18-20 A at 28 V.

2. Selection of the transistor

For a push-pull amplifier one can of course use two RF power transistors of the same type, but Gemini transistors – two transistors in the same package – are preferred for ease and compactness of building. They are readily available, and their characteristics are more closely matched than two independent devices, so they provide better amplifier symmetry. This table lists some Gemini transistors capable of at least 200 W RF power.

Reference	Manufacturer	Supply voltage (V)	Output power (W)	Gain (dB)	Efficiency (%)
BLF248	Philips	28	300	13	67
BLF278	Philips	50	300	16	55
BLF368	Philips	32	300	13,5	62
MRF141G	Motorola	28	300	14	55
MRF151G	Motorola	50	300	16	55
D1028UK	Semelab	28	300	13	60
DU28200M	M/A-COM	28	200	13	62
SD2932	STM	50	300	16	60
SR401	Polyfet	28	300	13	55

I chose 28V operation as that can easily be achieved, for example by putting two 13.8V power supplies in series, and there are also compact 28V SMPS (Switched Mode Power Supplies) available on the market nowadays. However, if you are about to build a dedicated power supply, it would be wise to select a 50V transistor, as these have more gain and are capable of better intermodulation (IMD) behaviour. Thanks to its availability and relatively cheap price, we selected the **MRF141G**.

3. Theory of operation

The amplifier is based upon a push-pull design. It consists of an input 0-180° phase splitter driving two identical active devices working in antiphase. At the output, the same 0-180° phase splitter is used as a combiner to deliver the output power of the two active devices to the amplifier load. The phase splitters are actually acting as transformers between the unbalanced coaxial input and output, and the balanced PA itself.

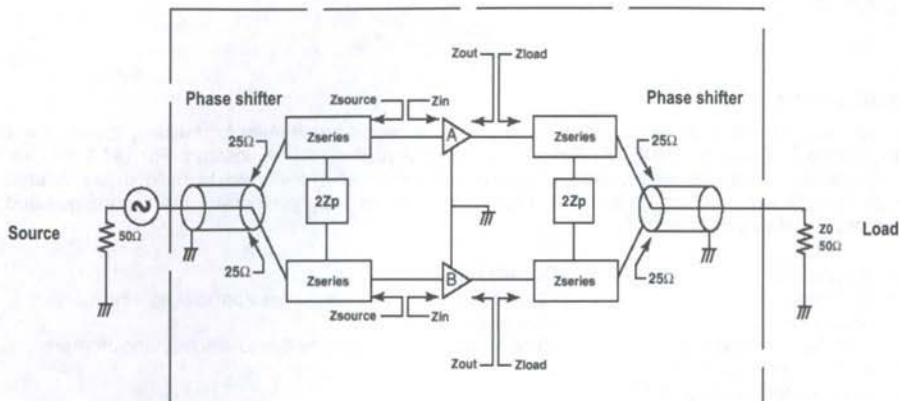


Fig. 1: Block diagram of a push-pull amplifier

Starting from the input source, the phase splitter delivers on its outputs both 0° and 180° phase shifted components of the input drive signal, together with converting the unbalanced 50Ω source impedance towards a $2 \times 25 \Omega$ balanced impedance. The purpose of the following network (Z_{series} and $2Z_p$) is to transform this 25Ω into the input impedance (Z_{in}) of blocks A and B, actually the active devices or transistors. Following these transistors, a similar network converts the $2 \times 25 \Omega$ balanced impedance of the output phase splitter/balun so that the transistors are each loaded by the complex conjugate (Z_{load}) of their output impedance (Z_{out}). In other words, the matching network will force the 25 Ω impedance to look like Z_{out}^* to the transistors ($Z_{load} = Z_{out}^*$). The transistors are operated in class B and each of them is conducting during alternate half-cycles.

4. Design of the amplifier

4.1. MOSFET high-level theory

The transistor used here is a NMOS (N-channel enhancement mode) device, the physical structure of which is shown in Fig. 2 below.

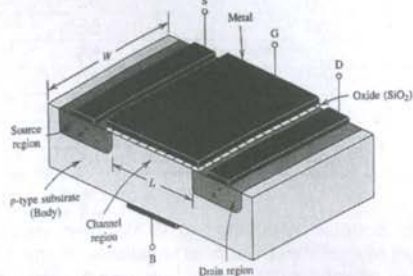


Fig. 2: Structure of a NMOS FET

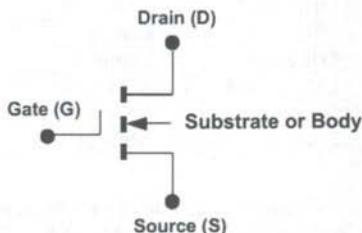


Fig. 3: Electronic symbol

With a positive voltage on the Drain (D) with respect to the Source (S), the Gate (G) must be biased to a positive voltage (again with respect to Source) to allow a Drain-Source current (I_d) to flow. This can be seen in Fig. 4.

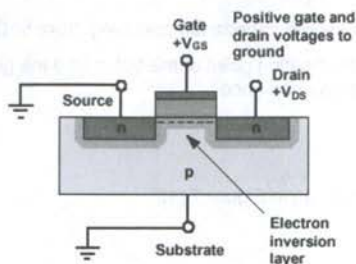


Fig. 4: Biasing of a NMOS FET

The minimum (threshold) value of the Gate-Source voltage which allows a D-S current to begin to flow is $V_{gs(th)}$. The value of $V_{gs(th)}$ is controlled during device fabrication and typically lies in the range 0.5 to 3 volts. Figure 5 below is the transfer characteristic of the device, and g_{fs} is the transconductance.

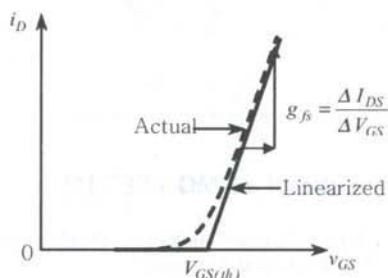


Fig. 5: Transfer characteristic

4.2. Baluns

The baluns are made of 50Ω coaxial cable having an electrical length of $\lambda/4$. The outer braid is grounded at only one end, the unbalanced termination, while the other end is floating and makes a balanced termination. Charge conservation requires that the currents on the centre conductor and on the outer braid maintain equal magnitude, and there is a 180° phase difference at any point along the line.

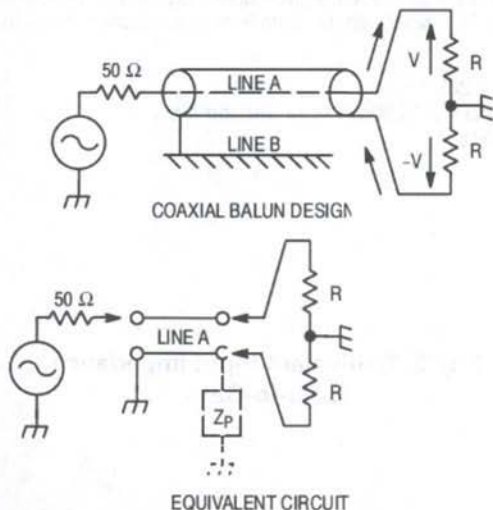


Fig. 6: Electrical schematic of the Baluns

Knowing the characteristic impedance of the Balun (Z_{balun}) to be 50Ω , we have:

$$Z_{\text{belun}} = \sqrt{50 \cdot 2 \cdot R} \Rightarrow R = 25 \Omega$$

So, by themselves, the baluns are already providing some impedance matching, from 50Ω to 25Ω.

Z_p in Figure 6 is the parasitic impedance between the floating point of the balun and the ground. This must be kept as high as possible ($Z_0 \gg R$) to avoid an unbalance.

4.3. Input and output impedances

The equivalent schematic of a single NMOS FET is given in Figure 7 [1]:

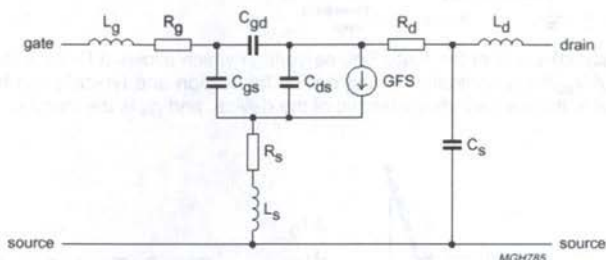


Fig. 7: Equivalent schematic of a NMOS FET [1]

All of the major and parasitic components shown in Figure 7 are embedded in models used by non-linear simulation tools, though only some of the values can be found in data sheets.

Regarding impedance matching, S-parameters are useless here as these are only valid for small signals, while we are operating here in large signals. Nevertheless, the **large signal** input and output impedances of the MRF141G can be extracted from its data sheet (see Appendix 1):

- $Z_{in} = (R_{in} + jX_{in}) \Omega = (1.20 - j1.50) \Omega$
- $Z_{load}^* = Z_{out} = (R_{out} + jX_{out}) \Omega = (3.90 - j0.85) \Omega$

These are Gate-to-Gate and Drain-to-Drain impedances, for a given operating voltage, bias, frequency of operation – and also for a particular resistor in parallel with the Gate (which is not often stated in the data sheet). The impedances are valid for:

- V_{dd} (Drain voltage) = 28V
- I_{dq} (quiescent current) = 2 * 250mA (see Section 4.5.)
- Frequency = 145 MHz

4.3.1. Input Impedance

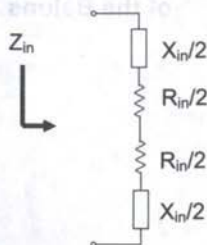


Fig. 8: Equivalent input impedance Gate-to-Gate

It is assumed the reactance given in the data sheet is a net one, i.e. resulting from both the reactance of the die (capacitive) and the inductive reactance due to the leads and bonding wires of the transistor. To perform the design, we consider **each side** (or die) of the transistor **individually** ("half") and we will

calculate the matching circuit for $Z_{in\ half} = \frac{R_{in}}{2} + j \frac{X_{in}}{2}$.

We then consider the input series impedance extracted out of the data sheet:

$Z_{in\ half} (\Omega)$	Equivalent series circuit
$0,60 - j0,75$	$0,60 \Omega + 1,46 \text{ nF}$

4.3.2. Output Impedance

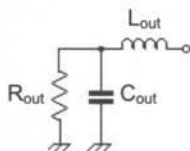
4.3.2.1 First Method

In a similar way as in Section 4.3.1., we derive the series output impedance out of the data sheet and, considering one side of the transistor, we get:

$Z_{out\ half} (\Omega)$	Equivalent series circuit
$1,95 - j0,42$	$1,95 \Omega + 2,60 \text{ nF}$

4.3.2.2 Second Method

Beside the input & output series impedances given in the data sheet, the equivalent (simplified) schematic of the output impedance of one side (die) of the transistor can be represented as follows:



$$R_{out} = R_{load} = \frac{(V_{dd} - V_{sat})^2}{2 * P_{out}} = \frac{(0,85 * V_{dd})^2}{2 * P_{out}}$$

$$C_{out} = 1,2 * C_{oss}$$

Fig. 9a: Equivalent parallel schematic for one die

$V_{dd} = 28\text{V}$, $P_{out} = 150\text{W}$ (per transistor die/side) and $C_{oss} = 420\text{pF}$ (per die).

The "1.2" multiplying factor (actually ranging from 1.15 to 1.3) in the calculation of C_{out} is an empirical factor due to the voltage swings that make C_{oss} varying, as indicated in some application notes [1].

L_{out} is assumed from figures found in data sheets and application notes.

By substituting in the equations, we get:

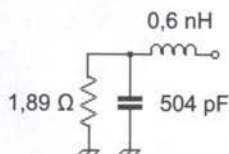


Fig. 9b

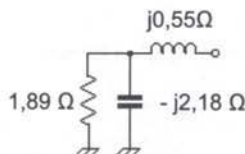


Fig. 9c

When using the equations given in Appendix 3 for parallel to series impedance transformation, we can derive the series equivalent schematic (valid only at the same frequency):

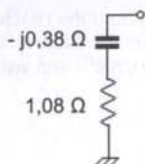


Fig. 10: Equivalent series schematic for one die

4.3.2.3 First versus Second Method

As a summary of the two methods, we have:

Method	$Z_{out\ half} (\Omega)$	Equivalent series circuit
First	$1,95 - j0,42$	$1,95 \Omega + 2,60\text{ nF}$
Second	$1,08 - j0,38$	$1,08 \Omega + 2,89\text{ nF}$

On a 25Ω normalized Smith chart, both impedances are relatively close to each other. From now on, we will work with the second method.

The topic of data sheet impedances, impedances for conjugate match or for best efficiency and S-parameters has been extensively explained in [2].

4.4. Synthesis of the matching networks

Since the transistor input & output impedances have been defined, the task of the designer regarding matching is shown below (still considering one die of the transistor) :

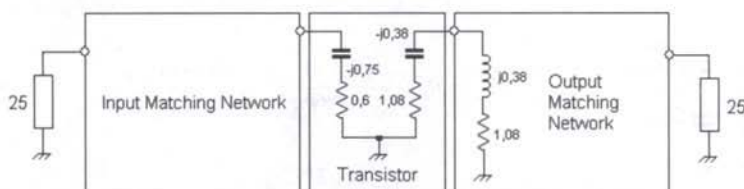
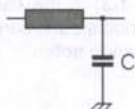
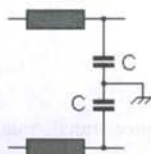


Fig. 11: Equivalent schematic of the input and output impedances

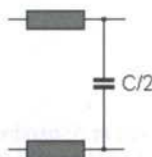
The impedance matching networks are made of low-pass filter sections (made of capacitors and printed striplines):



The two sides of the amplifier will be "merged" as follows:



which is equivalent to:



If the amplifier is well balanced, the currents flowing at the junction of both C capacitors are equal in amplitude and in opposite directions. That point is then acting as a **virtual ground**, so that the ground connection can be omitted and one capacitor (of half value) instead of two can be used.

The matching could be achieved by mean of a single low-pass matching section but this must be avoided. Because the input and output impedances of the transistor are very low, a single matching section would require a very high operating Q. High Q will lead to high circulating currents and hence high losses, together with potential instability and too narrow bandwidth. Therefore the matching should be achieved using several cascaded sections, each of which can have a more moderate working Q.

Though the synthesis of the matching networks can be done graphically "by hand" on a paper Smith chart, it is more straightforward to use computer software. The one used is **Smith V2.03** written by Fritz Dellsperger, HB9AJY [3].

For this design it is convenient to use a chart that is normalized to 25Ω , and the characteristic impedance of the matching striplines has also been set to 25Ω . There is an infinite number of possible solutions to "link" 25Ω (centre of the chart) to $Z_{in\ half}$ and $Z_{out\ half}^*$ but always keep in mind a low Q (Q curves can be drawn on the chart) is recommended while choosing the elements.

4.4.1. Synthesis of the input matching network

The input matching network transforms the transistor input impedance $Z_{in\ half} = (0.6 - j0.75)\Omega$ towards the $(25 + j0)\Omega$ impedance present after the input balun. In other words, the input matching network makes $Z_{in\ half}$ appear like a $(25 + j0)\Omega$ load to the input balun.

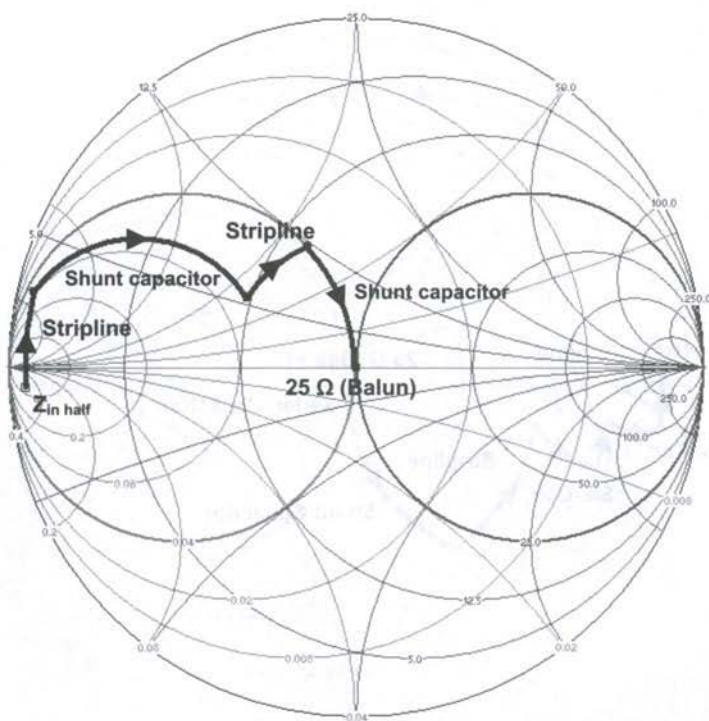


Fig. 12: Input matching network synthesis on the Smith chart

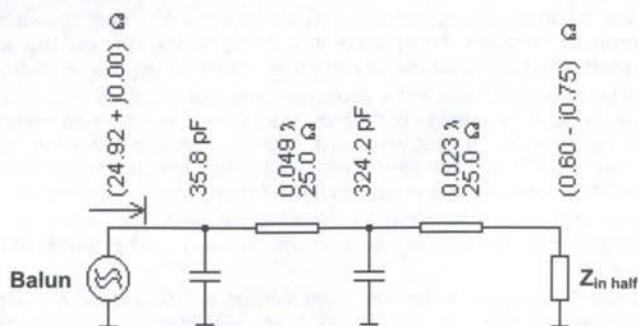


Fig. 13: Components of the input network (one side)

4.4.2. Synthesis of the output matching network

The output matching network transforms the $(25 + j0)\Omega$ impedance of the output balun into $Z_{out\ half}^*$ which is the complex conjugate of the transistor output impedance. The output matching network makes $(25 + j0)\Omega$ to appear like $Z_{out\ half}^*$ to the Drain of the transistor, so that the reactive parts of $Z_{out\ half}$ and $Z_{out\ half}^*$ cancel each other, while the resistive parts are equal and provide the most efficient power transfer.

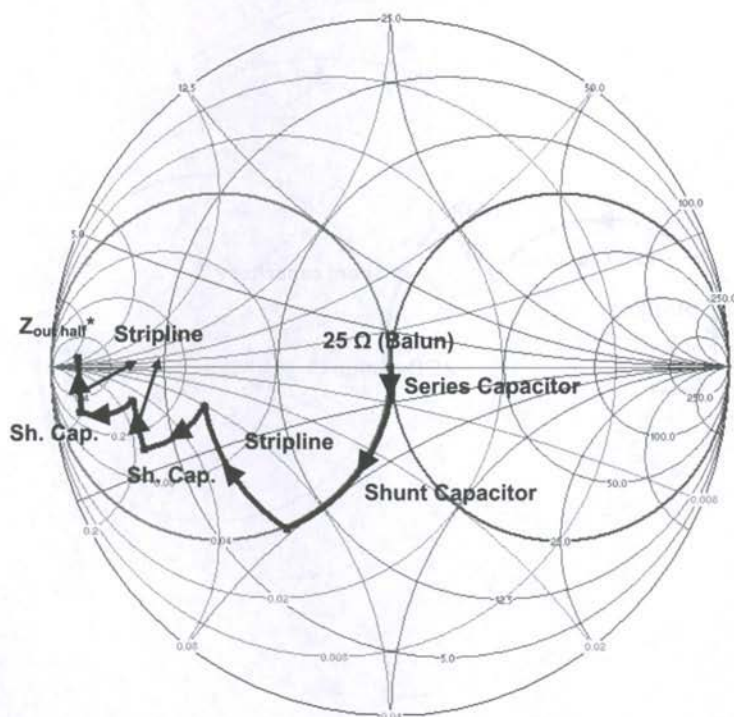


Fig. 14: Output matching network synthesis on the Smith chart

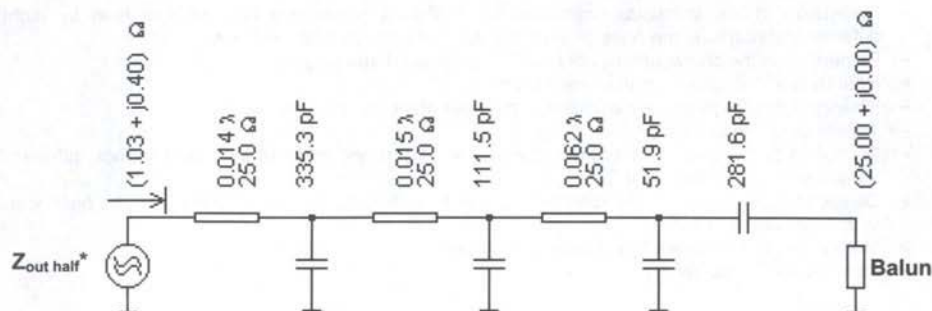


Fig. 15: Components of the output network (one side)

4.4.3. Comparison between actual and theoretical values

The amplifier was first built with the theoretical values obtained as above; but it was not delivering the expected output power, was exhibiting an efficiency lower than 50%, and had a poor input VSWR. The component values then had to be optimized.

The method used was simply "cut and try", which is not very scientific but I don't have any way to measure the actual transistor impedances, and don't have access to famous non-linear design software tools. The tables below indicate the differences between the theoretical component values and the actual optimized values.

Input Matching Network		
Component	Theoretical value	Actual value
Stripline	0,023 λ	0,023 λ
Shunt Capacitor	324 pF	324 pF
Stripline	0,049 λ	0,057 λ
Shunt Capacitor	36 pF	Variable 44 to 76 pF
Shunt Capacitor	-	10 pF at balun input (C24 on the RF board part list)

Output Matching Network		
Component	Theoretical value	Actual value
Series Capacitor	282 pF	282 pF
Shunt Capacitor	52 pF	52 pF
Stripline	0,062 λ	0,062 λ
Shunt Capacitor	112 pF	112 pF
Stripline	0,015 λ	0,015 λ
Shunt Capacitor	335 pF	300 pF
Stripline	0,014 λ	0,013 λ

The differences are highlighted in bold. We see that the values of the actual built amplifier are either the same as the theoretical design, or quite close. The small final changes make a big difference in performance, but the theoretical design was absolutely necessary to bring us to this place.

The difference in the input network can be explained by the fact the damping circuit (see Section 4.6) used for stability purpose introduces new components and hence modifies the impedance. It has also been found experimentally that adding a shunt capacitor of 10pF in front of the input balun (C24 on the RF board) improves the input VSWR.

From a general point of view, if an amplifier is not performing as expected (gain, efficiency, output power) according to the theoretical values of the matching networks' components, the reasons could be:

- Dispersion in the transistor characteristics (different production batches can lead to slightly different impedances, the ones given in the data sheets are average ones)
- Dispersion in the characteristics of the PCB (mainly printed striplines)
- Rounding of the figures on the Smith chart
- Rounding due to graphical derivation of data out of the data sheets
- Tolerance of the components
- According to the class of operation (conduction angle), the value of the load can look different to the transistor (see Section 4.5)
- Quiescent current (I_{dq}), Drain voltage (V_{dd}) and Gate-Source resistor different than the ones stated in the data sheet (if stated)
- Mutual coupling between the striplines (push-pull)
- Imperfection of the baluns.

4.5. Biasing of the amplifier

If the amplifier was operated in class A (small signal), the two dies inside the MRF141G conduct at the same time and the current flowing through each Drain is i . Given an impedance transformation ratio n (between the Drain and the load), the current flowing in the 50Ω output load (i_L) is:

$$i_L = \frac{2 * i}{n}$$

And the voltage (v_L) across this load is:

$$v_L = i_L * 50 = \frac{2 * i * 50}{n}$$

While the voltage on each Drain is:

$$v_d = \frac{v_L}{n}$$

And the load seen from the Drains is:

$$R_{dA} = \frac{v_d}{i} = \frac{v_L}{n * i} = \frac{2 * 50}{n^2}$$

When the amplifier is operated in push-pull class B, the Drain-to-Drain voltage swing is twice that of a single-ended class A amplifier. Only one of the two dies inside the transistor package is conducting (on alternate half-cycles, the other being blocked). So, the current flowing in the 50Ω output load is:

$$i_L = \frac{i}{n}$$

And the load seen from the Drains is:

$$R_{dB} = \frac{50}{n^2}$$

We then see that:

$$R_{dB} = \frac{R_{dA}}{2}$$

So, the load seen from the Drains in class B is half the one seen in class A. From an amplifier gain point (A_v) of view, we have:

$$\triangleright A_{V \text{ Small Signal}} = g_{fs \text{ Small Signal}} * R_{dA}$$

$$\triangleright A_{V \text{ High Signal}} = g_{fs \text{ High Signal}} * R_{dB} = g_{fs \text{ High Signal}} * \frac{R_{dA}}{2}$$

To be linear, the amplifier must have the same gain for small and large signals. Then:

$$A_{V \text{ Small Signal}} = A_{V \text{ High Signal}} \Rightarrow g_{fs \text{ Small Signal}} * R_{dA} = g_{fs \text{ High Signal}} * \frac{R_{dA}}{2}$$

We can conclude: $g_{fs \text{ Small Signal}} = \frac{g_{fs \text{ High Signal}}}{2}$

The amplifier has then to be biased so that the slope of the transfer characteristic without RF excitation (or $g_{fs \text{ Small Signal}}$) is half the high-signal slope ($g_{fs \text{ High Signal}}$). This avoids crossover distortion, as shown on the following picture:

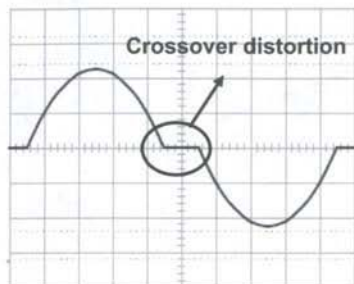


Fig. 16: Crossover distortion

The goal is then here to set up a Gate voltage (V_{gs0}) so that a quiescent current (I_{dq}) flows through each Drain.

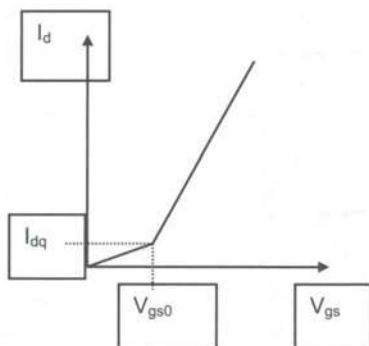


Fig. 17: Bias point on the transfer characteristic

A MOSFET Gate behaves like a capacitor at DC, thanks to its very high impedance. So, biasing the Gate requires very little current and a simple resistor voltage divider easily fulfils the requirement. Here is an extract from the schematic of the bias network (see Section 5.1.1 for more details).

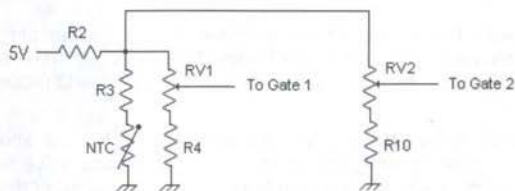
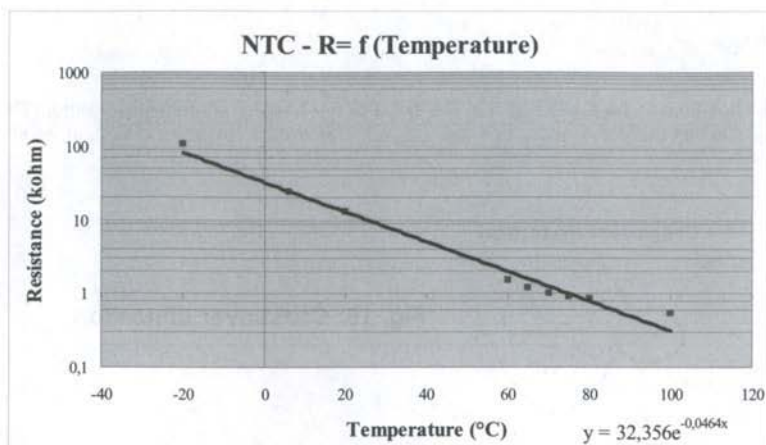


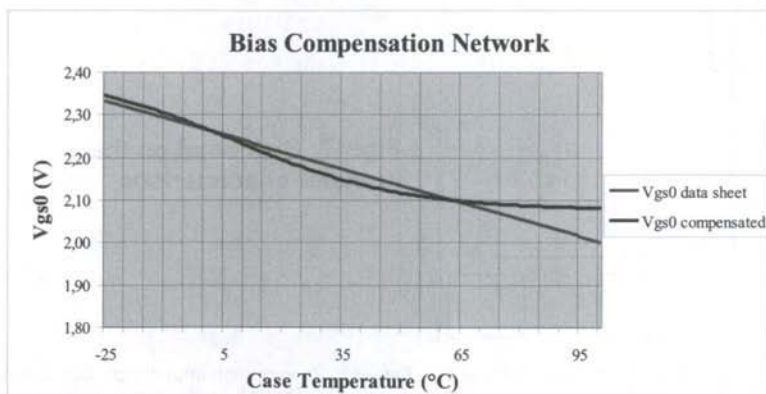
Fig. 18: Gate bias network

RV1 and RV2 are adjusted to get a quiescent current of 250mA through each Drain. This is achieved with a V_{gs0} around 2.2V on each Gate (@ 25°C).

The data sheet tells us that the V_{gs0} varies according to the case temperature of the transistor, so that some amount of temperature compensation is needed to keep a stable bias point. This is achieved by mean of a NTC (Negative Temperature Coefficient) resistor. I reused one from my junk-box; unfortunately it is unmarked, so I measured the NTC characteristic:



Knowing the value of the NTC according to the temperature, and having already fixed the values of all the components except R2 and R3, these last two values have been calculated (their ratio) so that the compensated V_{gs0} follows the same slope as V_{gs0} in function of the case temperature given in the data sheet. Obviously, both the case of the transistor and the NTC must be in close thermal contact.



4.6. Stability

No particular calculation has been done to assess the stability of the amplifier. Instead, a damping network (R15-C25-C26) has been added at the input (idea extracted from Philips data sheet [4]) and the Gate resistor (R7/R8) value has been carefully selected on test. Both methods help to damp the Q factor of the input network.

With the values shown on the schematic of the RF Board, the amplifier is stable, even if its input and output are left open-circuit (no load). If there is no input damping circuit, or if the Gate resistor value is above 10Ω, the amplifier runs into oscillation. A damping network has also been tried at the output of the amplifier but it turned out to be useless. From a general point of view, the solutions helping to stabilize a power amplifier are:

- Low Q matching networks (*)
- Damping of matching networks (*)
- Series or parallel Gate resistor (*)
- Drain to Gate feed-back.

Three of those methods (*) are used here.

4.7. Low-Pass Filter (LPF)

A 5-pole LPF has been added at the output of the amplifier to attenuate the harmonics and also those intermodulation (IMD) products that fall close to the harmonic frequencies. It is worthwhile to mention here that thanks to the Push-Pull configuration, the even-numbered harmonics ($2f$, $4f$...) and the even-order IMD products (f_1+f_2 , $2f_1+2f_2$...) are already well attenuated by the amplifier itself (if well balanced).

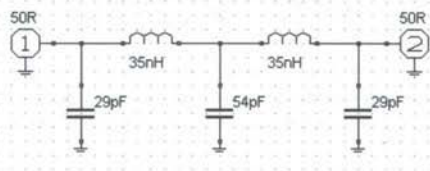


Fig. 19: Output Low-Pass Filter

The design of the filter has been conducted using the freeware **RFSim99** [5]. The transfer function (S21) and return loss (S11) are shown on the graph here after. The filter starts to cut-off a bit above 200 MHz.

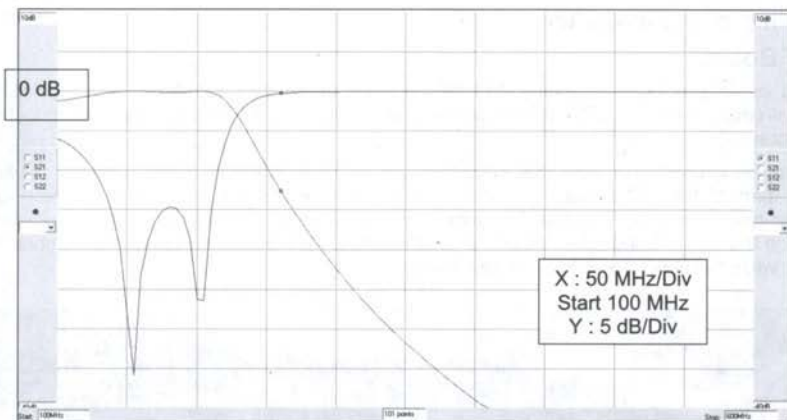


Fig. 20: Simulated transfer function of the LPF

There would still be room to move the cut-off closer to 150 MHz. However, the measurements done on the built LPF show that the out-of-band rejection is a few dB better than the simulated performance (the effect of the screen between the two band inductors was not simulated).

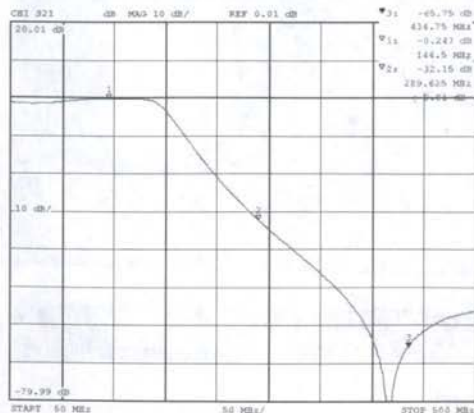


Fig. 21: Measured transfer function of the LPF

From the measurement (Fig 21), we get the table below:

Frequency	S21 (dB)	Remark
145	- 0,25	Fundamental (f_0)
290	- 32	2 nd Harmonic ($2*f_0$)
435	- 66	3 rd Harmonic ($3*f_0$)
580	- 52	4 th Harmonic ($4*f_0$)

The rejection of the 3rd Harmonic is 66 dB. This value would be decreased if the cut-off frequency were moved closer to 150 MHz, or if other self-resonant frequencies were introduced by using components of different value; so the design has been kept like it is. The return loss (S11) is better than 30 dB over the 2m band.

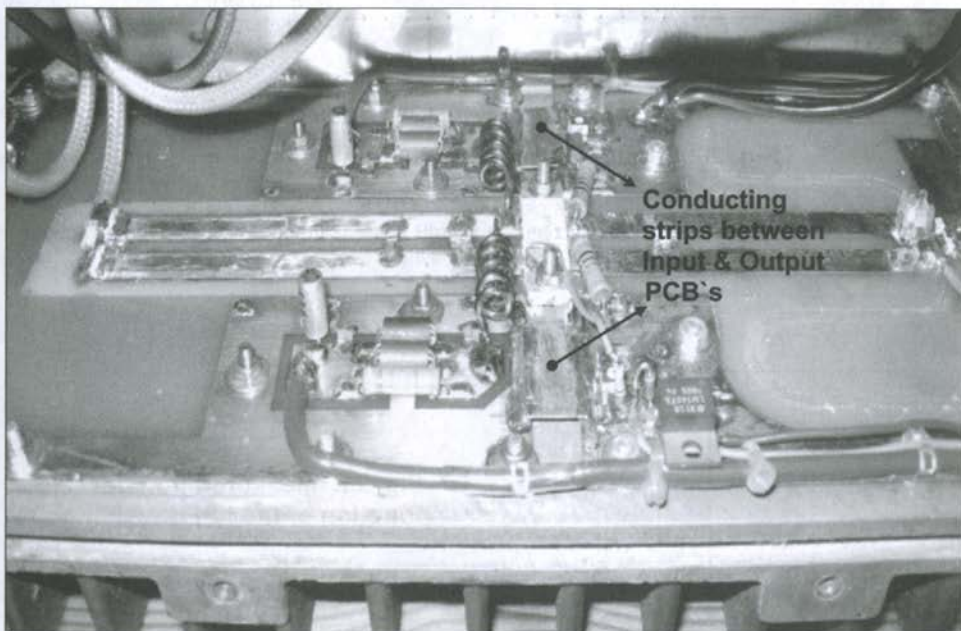
The LPF PCB also includes a basic directional coupler to assess the Direct (Dir.) and Reflected (Ref.) powers for output power monitoring purpose, and to supply the VSWR protection circuit. The coupling loss amounts to 30.6 dB on the coupled line.

5. Building of the amplifier

5.1. RF Board

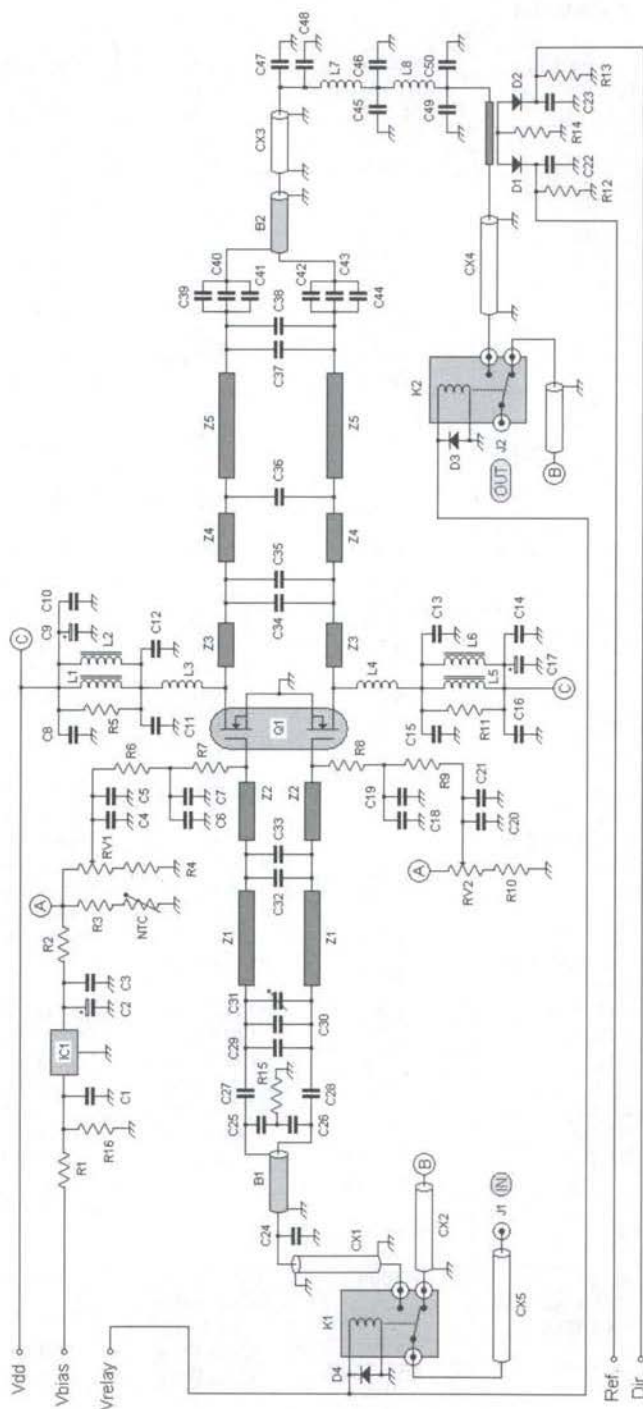
This "board" actually includes three different PCBs: an input board, an output board, and a small PCB with a directional coupler and the LPF. Where needed, the boards are bridged by copper conducting strips (see photographs).

Readers may be interested to know that the schematic has been drawn with only a simple drawing editor (MS Paint, part of the MS operating systems). A master file including the most common electronic symbols has been "manually" created. The schematics are then drawn by reusing that same common file and by using the "select" and "copy-paste" functions. Lines are then drawn to link the symbols between each other, while the unused symbols are just deleted.



RF Board

5.1.1. Schematic of the RF board



5.1.2. Parts list

Part ID	Value	Type	Supplier	Remarks
R1	1 k Ω	¼ W	Various	Through Hole
R2	4,7 k Ω	¼ W	Various	Through Hole
R3	20 k Ω	¼ W	Various	Through Hole
R4, R10	10 k Ω	¼ W	Various	SMD 1206
R5, R11	8,2 Ω	1 W	Various	Metal Film MR52
R6, R9	1 k Ω	1,6 W	Various	Metal Film PR37
R7, R8	10 Ω	1 W	Various	Metal Film MR52
R12, R13	1 M Ω	¼ W	Various	SMD 1206
R14	47 Ω	¼ W	Various	SMD 1206
R15	10 Ω	1 W	Various	Metal Film MR52
R16	10 k Ω	¼ W	Various	Through Hole
RV1, RV2	10 k Ω	3314 (¼ W)	Bourns	SMD
NTC	10 k Ω	@ 25°C – See section 4.5.		
C1, C5, C7, C10, C12, C13, C14, C19, C21, C22, C23	1 n	X7R	Various	SMD 1206
C2	1 μ	Tantalum 16V	Various	SMD
C3, C4, C6, C8, C11, C15, C16, C18, C20	100 n	X7R	Various	SMD 1206
C9, C17	10 μ	Electrolytic 50 V	Various	Through Hole
C24	10 p	NP0 500V	Philips	R100G19COGL (1)
C25, C26	27 p	P100 Porcelain	Temex (Hi-Q)	500CHB270FV
C27, C28	1 n	P90 Porcelain	ATC (100B)	ATC100B102KW500
C29	4,7 p	P100 Porcelain	Temex (Hi-Q)	500CHB4R7BV
C30	15 p	NP0 500V	Philips	R150G19COGL
C31	2-18 p	PTFE dielectric film	Philips	2222 809 05217
C32	150 p	P90 Porcelain	ATC (100B)	ATC100B151JW500
C33	12 p	P100 Porcelain	Temex (Hi-Q)	500CHB120FV
C34, C39, C44	82 p	P100 Porcelain	Temex (Hi-Q)	500CHB820FV
C35	68 p	P100 Porcelain	Temex (Hi-Q)	500CHB680FV
C36	56 p	P100 Porcelain	Temex (Hi-Q)	500CHB560FV
C37	18 p	P100 Porcelain	Temex (Hi-Q)	500CHB180FV
C38	8,2 p	P100 Porcelain	Temex (Hi-Q)	500CHB8R2BV
C40, C41, C42, C43	100 p	P100 Porcelain	Temex (Hi-Q)	500CHB101FV
C47, C50	6,8 p	P100 Porcelain	Temex (Hi-Q)	500CHB6R8BV
C48, C49	22 p	P100 Porcelain	Temex (Hi-Q)	500CHB220FV
C45	15 p	P100 Porcelain	Temex (Hi-Q)	500CHB150FV
C46	39 p	P100 Porcelain	Temex (Hi-Q)	500CHB390FV
L1, L2, L5, L6		VK200 Choke	Philips	
B1, B2		N/4 Balun	Home	See section 5.1.3.
D1, D2	5082-2811	Schottky	Agilent (HP)	Through Hole
D3, D4	1N4148		Various	Through Hole
Q1	MRF141G		Motorola, Tyco Electronics, M/A-Com	(2)
IC1	7805	5V Regulator	Various	
CX1, CX2, CX3, CX4, CX5	RG 400	Coax cable sections	Huber&Suhner	
K1	CX120A	Coax Relay	Tohtsu	
K2	CX520D	Coax Relay	Tohtsu	

J1	Female N	Connector	Various	On Front-Panel		
J2	Female N	Connector	Various	Part of K2 (CX520D)		
Homemade Inductors' data						
	Value	Internal Ø	Wire Ø	Length	Winding	# Turns
L3, L4	≈ 35 nH	5 mm	1,5 mm	17 mm	Spaced	4,5
L7, L8				14 mm, mounted 5 mm above PCB		3,5
Stripline data						
	Length (mm)	Width (mm)	El. Length (λ)	Remarks		
Z1	61,0	7,5	0,057	0,3mm th., 5mm wide CuAg strip soldered on PCB stripline		
Z2	23,5		0,023			
Z3	14,0		0,013			
Z4	16,0		0,015			
Z5	68,0		0,062			
PCB's: 1.6mm thick, double sided FR4 epoxy glass fibre (ε _r = 4.6)						

(1): Experimentally, it has been found this capacitor improves the input Return Loss.

(2): Can be bought at RF Parts (<http://www.rfparts.com>) in the USA. ASI Advanced Semiconductor Inc (<http://www.advancedsemiconductor.com>) is also selling the MRF141G.

5.1.3. Baluns

The input Balun is made of RG 316 PTFE dielectric 2,5 mm O.D. coaxial cable manufactured by H&S. The output Balun is made of RG 400 cable of the same manufacturer. The velocity factor (V_f) of both cables is 0,695.

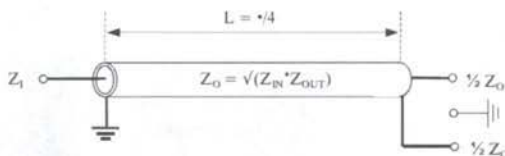


Fig. 22: Drawing of the Baluns

Both cables have an electrical length of $\lambda/4$, and the velocity factor (V_f) of both cables is 0.695.

This leads to a physical length of $\frac{300}{145} * 0,25 * V_f = 36 \text{ cm}$

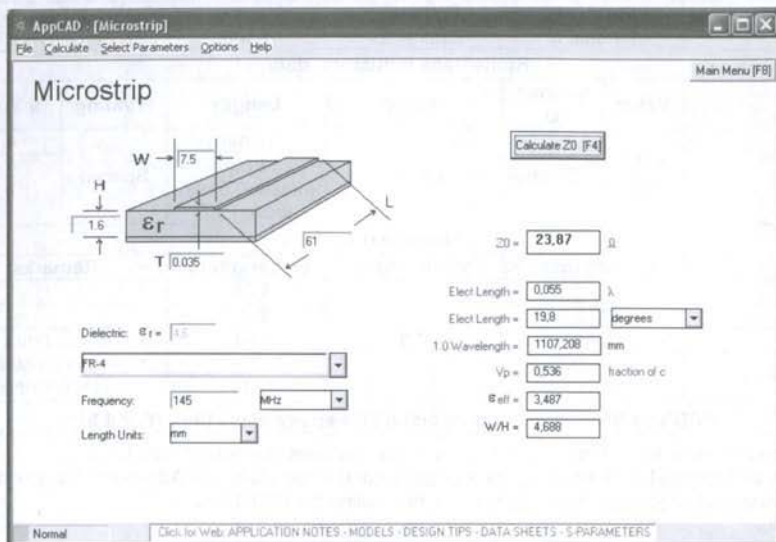
Make them a little bit longer to allow the solder junctions with the matching striplines. Both baluns are wound as shown on the pictures (see Section 8). The winding diameter amounts to around 50 mm. As can be noticed on the same pictures, $\lambda/8$ printed baluns with semi-rigid cable were initially used but without too much success.

Note: Huber and Suhner is no longer manufacturing the RG316 or RG400, but the Enviroflex 316 and 400 instead. These cables have slightly different characteristics.

5.1.4. Matching striplines and PCBs

The three PCBs comprising the RF board are made of double-sided FR4 epoxy glass fibre. All PCB's are screwed directly onto the heatsink. When it is all about high currents and low impedances, ground continuity is very important, also for stability of the amplifier. Apart from the RF tracks, the layout is not critical. The two sides of the boards are linked together by copper strips all around the edges (Cu foil is easily available from the external "braid" of a piece of H100 coax cable) and also by as many through-board "vias" as possible. The input and output PCBs are also linked together by copper strips along both sides of the Gemini transistor package. The pictures of Section 8 are self-explanatory.

The striplines have been designed using the freeware **AppCAD** [6] from Agilent. Here is an example :



The constructional data of the critical RF tracks are shown on the pictures below :

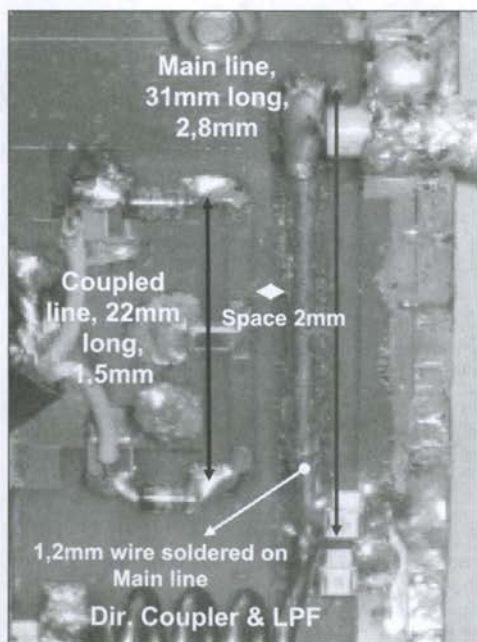


**Fig. 23: Directional coupler:
RF tracks details**

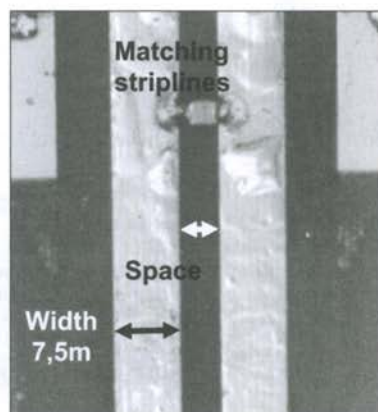


**Fig. 24: Matching
striplines details**

5.1.5. Cooling

The aluminium heatsink has been recycled from a military surplus power supply (see pictures in Section 8). No heat transfer calculation has been done, but the heatsink turned out to be big enough to allow SSB/CW operation without any extra cooling (at room temperature). When it is hot – and remember, this amplifier is designed to be operated outdoors, of course protected against rain but in a non air-conditioned environment – or indeed for heavy-duty operation, a snail blower provides more than enough cooling. Even during long periods of operation, the heatsink stays at room temperature.

The transistor is screwed onto a 1 mm thick piece of copper, acting as a heat spreader. The heat spreader is itself in close contact (screwed) with the heatsink.

To avoid mechanical stress due to temperature changes, it is normally recommended to bend the transistor leads. However, it hasn't been done here: the transistor leads have been kept straight and soldered directly to the PCBs, with no problems.

5.2. Control board

This board supervises the amplifier. It has been constructed using perforated matrix board with holes surrounded by copper pads on a 0.1-inch (2.54 mm) grid.

Once S1 (front-panel) is set to "ON" and S2 (front-panel) is set to "Operate", the amplifier is ready. In RX, the green LED D6 lights on the front panel. When the PTT input is grounded, the amplifier goes to TX mode; this is indicated by the red LED D5. The amplifier is sequenced to avoid "hot" switching of the coax relays K1 and K2 (RF Board) when RF is present. RV2 and C7 introduce a further time delay so that the bias is only applied to the transistor AFTER the K1 and K2 have been switched to TX (Normally Open position of the coax relays).

The operational amplifiers IC2A and IC2D shape the voltage out of the directional coupler (LPF PCB) to drive the TH1 thyristor that is the heart of the VSWR protection circuit. RV3 sets the VSWR threshold above which the amplifier goes into protection. In the protection mode, the amplifier goes into RX mode (bias is disabled and the coax relays go back to Normally Closed state). The thyristor latches the amplifier in protection mode until the "Reset" push button (front-panel) is pressed – which should not be done until after the VSWR fault in the antenna line has been found. IC2B amplifies the voltage sampled out of the direct power by the directional coupler. This voltage is approximately proportional to the square root of the output power. It could be displayed on a front-panel meter; but for my own station, where the amplifier is 50m away from the shack, a "Monitor" output jack has been provided so that the proper working of the amplifier can be monitored remotely. I use a simple LED that varies in brightness according to the RF output power; or alternatively a voltmeter can of course also be used.

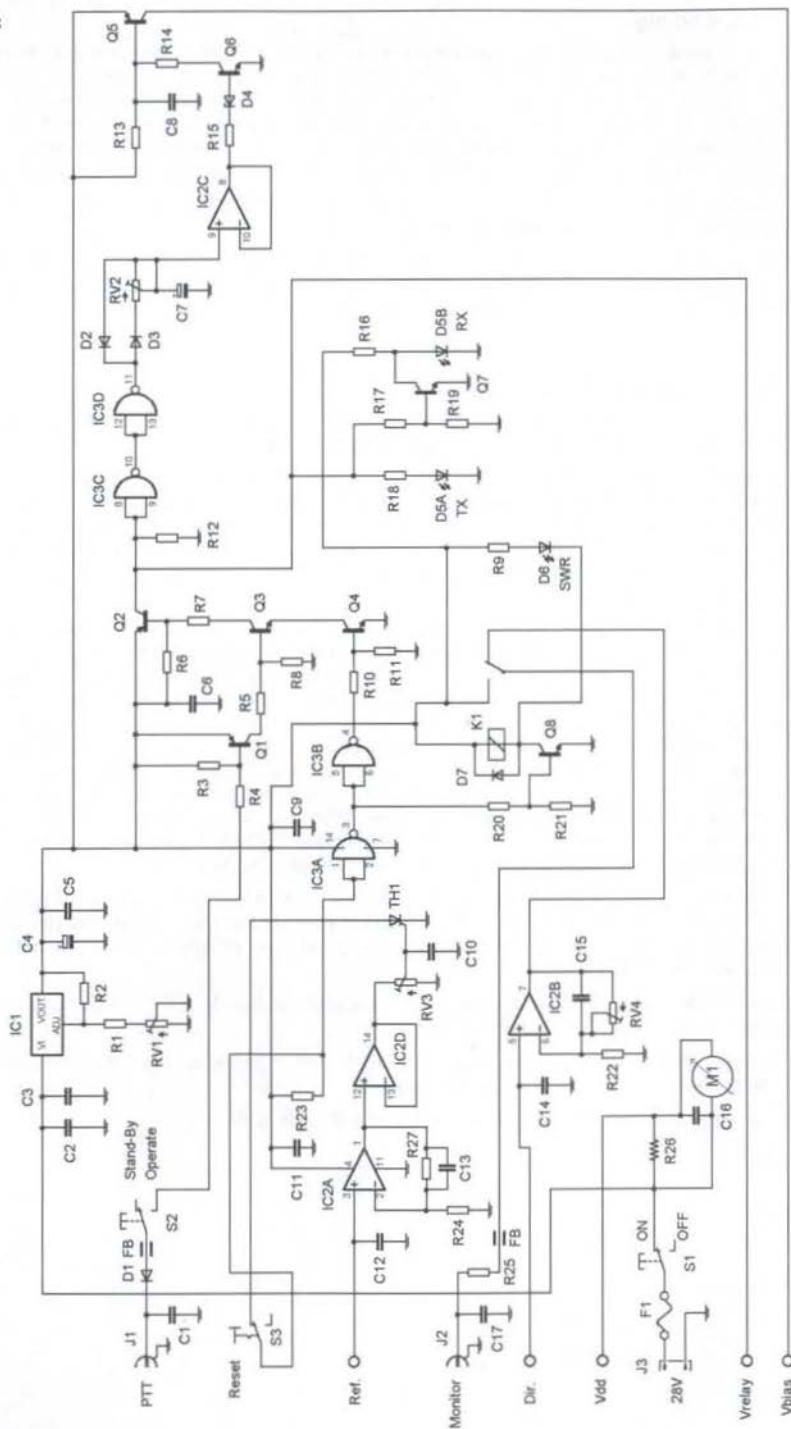
RV4 sets the maximum voltage on the "Monitor" output in normal operation. If the amplifier goes into protection due to bad VSWR, the relay K1 switches, so that the monitor voltage goes to high state until the "Reset" button is pressed. This can serve to activate an alarm; in the present case, the monitoring LED lights at full brightness.

The **VSWR protection is mandatory**, the transistor can handle a 5:1 VSWR but a short or an open in the antenna line makes the VSWR to be infinite...

R26 is a shunt resistor (75 mV drop under 30 A) that, together with the M1 meter, indicates (on the front-panel) the Drain current drawn by the transistor.

The schematic here has been drawn with **EAGLE Light Edition** [7].

5.2.1. Schematic of the Control board



5.2.2. Parts List

As this is a low frequency board, the package of the components (through hole or SMD) is not critical, and is not mentioned in the table below.

Part ID	Value	Type	Supplier	Remarks
R1	1,6 k Ω	$\frac{1}{4}$ W	Various	
R2	237 Ω	$\frac{1}{4}$ W	Various	Tolerance 1%
R3, R4	3,3 k Ω	$\frac{1}{4}$ W	Various	
R5, R15, R17, R20, R21	2,2 k Ω	$\frac{1}{4}$ W	Various	
R6, R8, R11, R19	10 k Ω	$\frac{1}{4}$ W	Various	
R7, R9, R14, R18	1 k Ω	$\frac{1}{4}$ W	Various	
R10, R13	4,7 k Ω	$\frac{1}{4}$ W	Various	
R12	47 k Ω	$\frac{1}{4}$ W	Various	
R16, R23, R25	820 Ω	$\frac{1}{4}$ W	Various	
R22	220 k Ω	$\frac{1}{4}$ W	Various	
R24	100 k Ω	$\frac{1}{4}$ W	Various	
R26	2,5 m Ω	Shunt Resistor, 75 mV drop at 30 A		
R27	1 M Ω	$\frac{1}{4}$ W	Various	
RV1	2,2 k Ω	$\frac{1}{2}$ W	Various	
RV2	50 k Ω	$\frac{1}{2}$ W	Various	
RV3	10 k Ω	$\frac{1}{2}$ W	Various	
RV4	1 M Ω	$\frac{1}{2}$ W	Various	
C1, C2, C6, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17	1 n	X7R	Various	
C3, C5	100 n	X7R	Various	
C4	15 μ	Electrolytic 50 V	Various	
C7	1 μ	Tantalum 16V	Various	
D1, D2, D3	1N4148		Various	
D4	9,1 V	BZX79C Zener diode	Philips	
D5	Dual color LED	Red/Green	Various	On Front-Panel
D6	LED	Red	Various	On Front-Panel
TH	2N5064	Thyristor	Various	
Q1	2N2907	PNP	Various	
Q2	BD676	Darlington PNP	Various	
Q3, Q4, Q6, Q7, Q8	BC109	NPN	Various	
Q5	2N2904	PNP	Various	
IC1	LM317T	Volt. regulator	Various	
IC2	LM324	AOP	Various	
IC3	HEF4011BD	NAND gates	Various	
K1	DO12-M	12V relay	Fujitsu	Any small relay is OK
S1	Switch	SPDT	Various	10 A handling, Front-Panel
S2	Rotary switch	At least 2 positions	Various	On Front-Panel
S3	Push button	Norm. Closed	Various	On Front-Panel
M1		Drain current meter	Various	Sold with shunt resistor (R26) – 6,8 mA for full scale deviation, 11 Ω internal resistor
F1	25A	Car fuse	Various	
J1, J2	RCA Jack	Connector	Various	On Front-Panel
J3		Power Connector	Various	On Front-Panel
FB	Ferrite bead		Various	
PCB	perforated	board		

6. Commissioning

This section describes the steps to be achieved in order to set the amplifier up and running.

1. Set RV1 of Control board so that its "hot" end (the one linked with R1) is connected to ground.
2. Set RV1 and RV2 of RF board so that the slider is set to the "cold" ends (the ends linked with R4 and R10 respectively). Short-circuit R4 and R10 of the RF board to ground (the MRF141G is cut off).
3. Set the slider of RV3 of the Control board to the "cold" end (ground).
4. Slowly adjust RV1 to get 13V at the output of the LM317 (IC1). Be careful not to exceed 15V for the safety of IC3.
5. Without any RF drive applied, set the PTT input (J1 of Control board) to ground back and forth, while adjusting RV2 of the Control board so that V_{bias} (collector of Q5 on the Control board) only rises AFTER the coaxial relays have been switched.
6. Disconnect CX3 from the RF board from the amplifier's output PCB and terminate it with a 50Ω load (min 10W). Mechanically switch K2 of the RF board and inject 8W of RF power on J2 (front-panel) of the RF board. Then, adjust RV3 of the Control board so that the front-panel "VSWR" LED lights. This sets the VSWR protection threshold. At full output power (300W), a reflected power of 8W corresponds to a 1.4:1 VSWR. Remove the 50Ω load and re-connect CX3 on the output PCB of the RF board.
7. Connect a wattmeter and a high-power 50Ω load (> 300W) to J2 of the RF board. Connect a transceiver to J1 of the RF board, through a VSWR/watt-meter. Link the transceiver's PTT output to J1 of the Control board. Set the transceiver power output to 3W and key it. Adjust C31 of the RF board (with an insulated screwdriver) to achieve the best possible input VSWR while checking the output power. Around 100W of output power must be obtained. Slowly increase the transceiver power while re-adjusting C31 to keep a good input VSWR. The worst VSWR is 1.3 at mid drive power. At low and full drive, the VSWR-meter needle doesn't deviate at all. With 13W of drive power, the output power should be around 300W, together with a 50% efficiency. Below 300W, it is normal that the efficiency is worse. Due to the dispersion of the characteristics of the components (compared to the ones used here), perfect matching probably won't be achieved at first try. Extra tuning of the capacitors in the matching networks would then be required. This will be achieved by temporarily soldering variable capacitors instead of, or in parallel with the ones already in place. Capacitors of the same type as C31 will do the job.

Tuning is an iterative process. Start at low drive power levels and tune the output matching network, from the transistor to the output, back and forth. Then, tune the input network the same way. Afterwards, come back to retuning the output network. Continue carefully, at gradually increasing drive levels up to the maximum.

8. Adjust RV4 of the Control board to obtain the wanted monitor output voltage on J2 of the Control board.

7. Performance

Due to lack of measurement equipment, the performance assessment has been quite limited. However, at least the input/output power characteristic has been measured, as seen here:

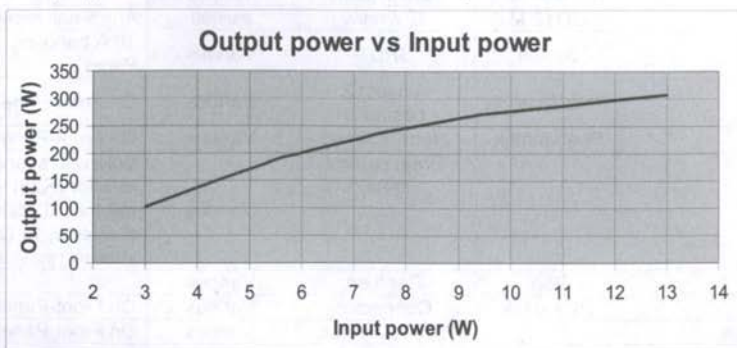


Fig. 25: Output power versus input power

The mean **gain** is **15 dB** and the **1 dB compression point** lies at **280W** output power. Although the intermodulation products and harmonic rejection have not been measured, the following picture, extracted from a Motorola application note [8], shows the harmonic rejection of a **broadband** amplifier (no output filtering) using the MRF141G. One clearly sees that at low frequencies, the push-pull configuration shows the even harmonics already well rejected (without any LPF) by the amplifier of its own, while the odd harmonic levels remain quite high. However, the falling gain at UHF means that at 144 MHz, the worst harmonic level is -45 dBc (third harmonic). Assuming the amplifier described here behaves the same way as the broadband one (which is unlikely to occur, thanks to the narrowband nature of the present amplifier, and the matching networks made of LPF sections) and then including the rejection provided by the output LPF, a (theoretical) **minimum harmonic rejection of 77 dBc** can be expected for all orders.

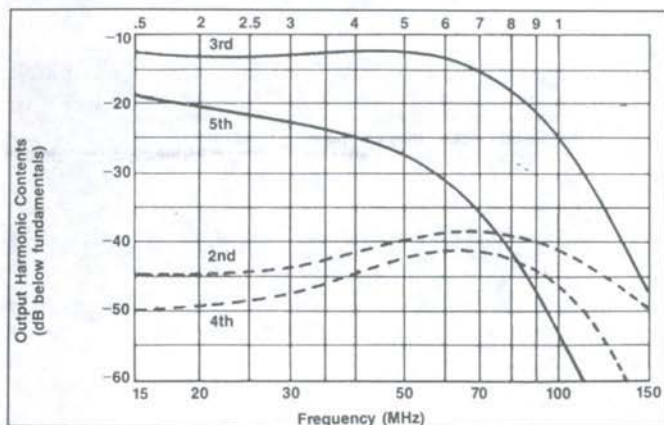


Fig. 26: Harmonic content of a broadband MRF141G

From a very subjective point of view, excessive splattering has never been reported, even by nearby stations. The current drawn to achieve full output power lies around **20A at 28V**, yielding an **efficiency of 53%**.

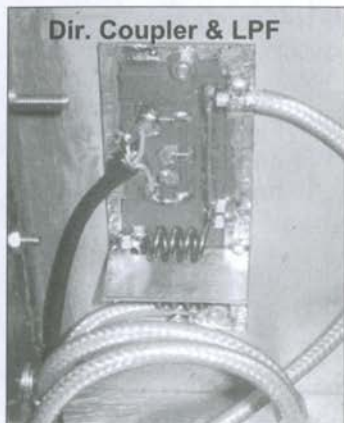
8. Pictures

This section shows in pictures some further constructional details of the amplifier.

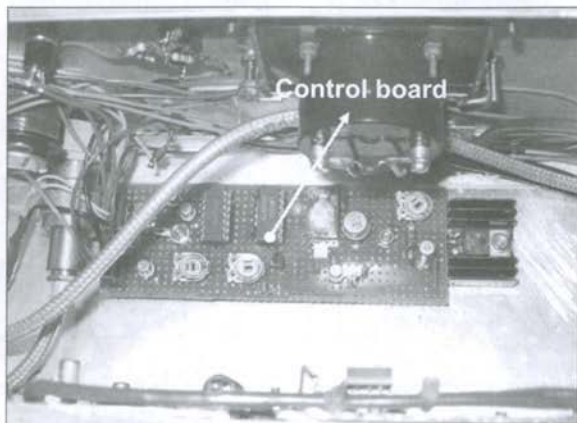




Dir. Coupler & LPF



Control board



Overall top view

